

## CLAIMS

*What is claimed is:*

*Sub A/2*

1. An active pixel sensor circuit comprising:  
a photodetector;  
an access transistor connected to the photodetector;  
an amplifier transistor connected to an output of the access transistor  
and to a signal output bus; and  
a reset transistor connected between the access transistor and the  
amplifier transistor, wherein the reset transistor is reset with a tapered reset signal.

2. The circuit of Claim 1, wherein the transistors are MOSFETs of identical  
polarity.

3. The circuit of Claim 2, further comprising a first column buffer connected  
to the reset and amplifier transistors.

4. The circuit of Claim 3, further comprising a second column buffer  
connected to signal output bus.

5. The circuit of Claim 4, further comprising a row disable transistor  
connected to the reset transistor.

6. The circuit of Claim 5, wherein the first column buffer, second column  
buffer and row disable transistor are connected to a plurality of active pixel sensor  
circuits.

7. The circuit of Claim 6, wherein the amplifier transistor operates as a driver  
of a source follower amplifier when a signal from the photodetector is being read out  
on a row-by-row basis, and operates as a driver of a reset amplifier when the  
photodetector is being reset.

8. An active pixel sensor circuit comprising:

2 photodetector means for converting light into an electrical signal;  
3 amplifier means for amplifying the electrical signal;  
4 access means for transferring the electrical signal from the  
5 photodetector means to the amplifier means;  
6 reset means for resetting the photodetector; and  
7 tapered reset signal means for applying a tapered reset signal to the  
8 reset means.

1 9. A method for low noise image formation in an active pixel sensor, the  
2 method comprising:

3 reading a signal on a photodetector;  
4 transferring the signal from the photodetector to an amplifier;  
5 reading out the signal from the amplifier to a bus; and  
6 applying a tapered clock signal to a reset transistor in order to reset the  
7 photodetector.

1 10. A CMOS imager array comprising a plurality of pixels, each pixel  
2 comprising:

3 a photodetector;  
4 an access MOSFET having a source connected to the photodetector;  
5 an amplifier MOSFET having a gate connected to a drain of the access  
6 MOSFET, a source connected to a signal bus, and a drain connected to a column  
7 buffer; and  
8 a reset MOSFET having a source connected to the drain of the access  
9 MOSFET, a drain connected to a column buffer, and a gate connected to a tapered  
10 reset signal generator.

1       11. The imager array of Claim 10, further comprising a row disable MOSFET  
2       having a source connected to the drain of the reset MOSFET and a drain connected to  
3       a row disable signal generator.

1       12. The imager array of Claim 11, further comprising an access signal  
2       generator connected to the gate of the access MOSFET.

1       13. The imager array of Claim 12, further comprising a column buffer  
2       connected to the signal bus.

1       14. The imager array of Claim 13, wherein the MOSFETs within each pixel  
2       are of identical polarity.

1       15. The imager array of Claim 14, wherein the photodetector comprises a  
2       substrate diode with the silicide cleared.

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